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Over 100 Million Frames per Second 368 Frames Global Shutter Burst CMOS Image Sensor with In-pixel Trench Capacitor Memory Array

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ABSTRACT

In this paper, a prototype ultra-high speed global shutter CMOS image sensor with in-pixel trench capacitor memory array achieving over 100M frames per second with up to 368 record length by burst CDS operation is demonstrated.

INTRODUCTION

Ultra-high speed (UHS) imaging technologies with over 100M frames per second (fps) high frame rate and longer record length is desired for the elucidation of UHS phenomena. Multi-framing cameras or streak cameras have been utilized in UHS imaging over 100Mfps[1]. UHS image sensors achieving over 100Mfps is highly desired for a simpler camera system. Burst CMOS image sensor technology is a candidate to achieve such high frame rate and high resolution with acceptable power consumption. Figure 1 shows structures of burst CMOS image sensors, where (a) shows the previously developed chip with memory array placed on the periphery of pixel array achieved 20Mfps with up to 256 record length[2,3], (b) shows an improved structure of (a) increased number of pixels and record length by high density memory array[4,5], (c) shows a planar structure with in-pixel high density memory array[6–8]. Recently, we have developed a prototype CMOS image sensor of Fig. 1(c) with conventional planar MOS capacitor memory array[7, 8]. It is mimicking a 3D stacked structure with pixel-wise interconnections for analog memory array placed beneath each photo-sensing cell[9] shown in (d). It achieved over 100Mfps with up to 80 frame video capturing by introducing the burst CDS technique[8] which can minimize the frame period.

A high density memory integration is the key technology to achieve all the structures in Fig. 1 (b–d) with a sufficient number of record length. The thermal noise arising at the memory capacitors is one of the dominant noise sources in this type of image sensors, thus a large capacitance value is required. Low leakage current and high uniformity are also required in order to maintain signal integrity. In order to meet such requirements, we have developed Si trench capacitor with improved effective capacitance area[4,5]. It achieved the capacitance density of 30fF/μm^2. The developed prototype image sensor realized 10Mfps UHS imaging with 960 record length with half pixel mode[5].

In this work, we developed a burst CMOS image sensor with in-pixel trench capacitor memory array to

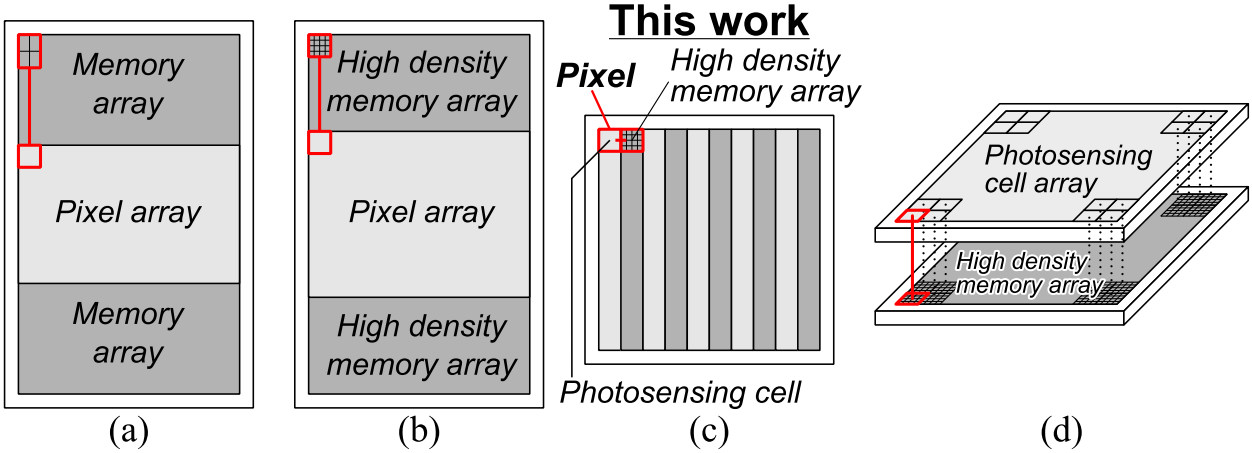


Figure 1 Schematic illustration of structures of burst UHS CMOS image sensor with on-chip memories; (a) the previously developed chip, (b) an improved structure of (a) with high density memory array, (c) a planar structure with in-pixel high density memory array, and (d) a backside illuminated 3D stacked structure with pixel-wise interconnections.

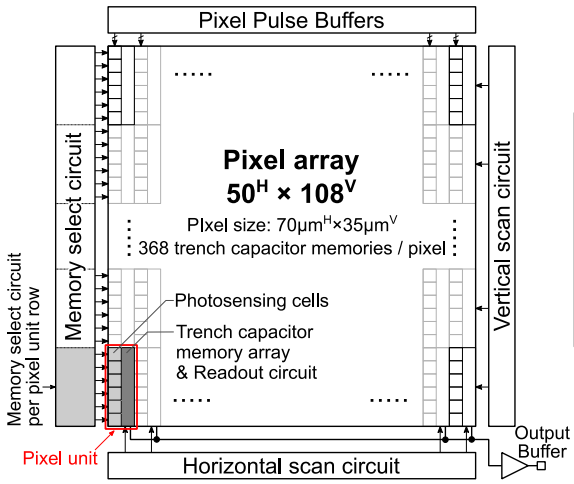


Figure 2 The block diagram of developed burst CMOS image sensor with in-pixel trench capacitor memory array.

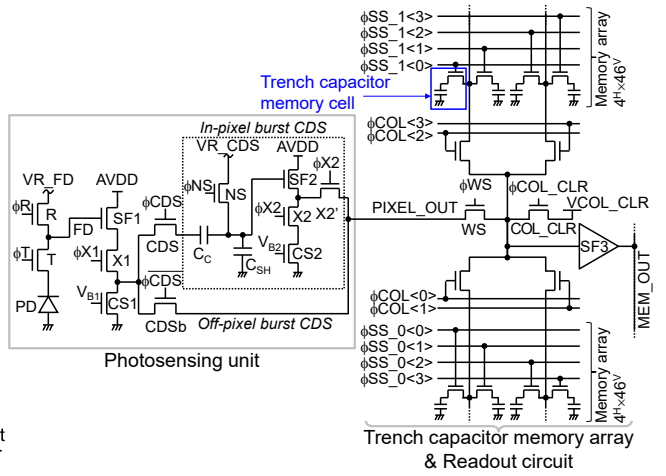


Figure 3 Pixel circuit schematic of the developed burst UHS CMOS image sensor.

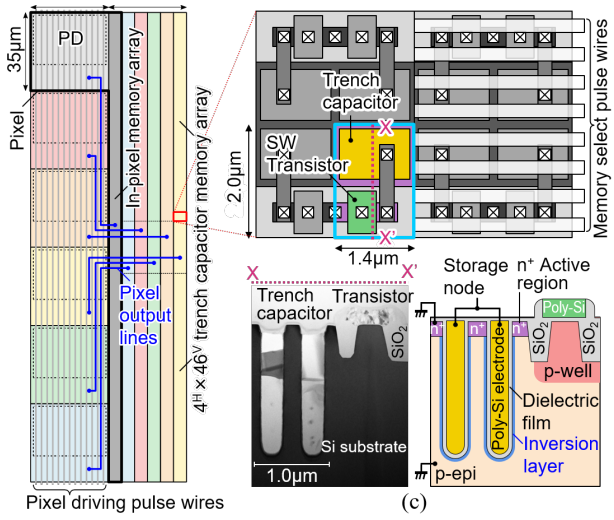


Figure 4 (a) Pixel arrangement of the developed image sensor, (b) layout diagram and (c) cross sectional diagram of the developed trench capacitor memory.

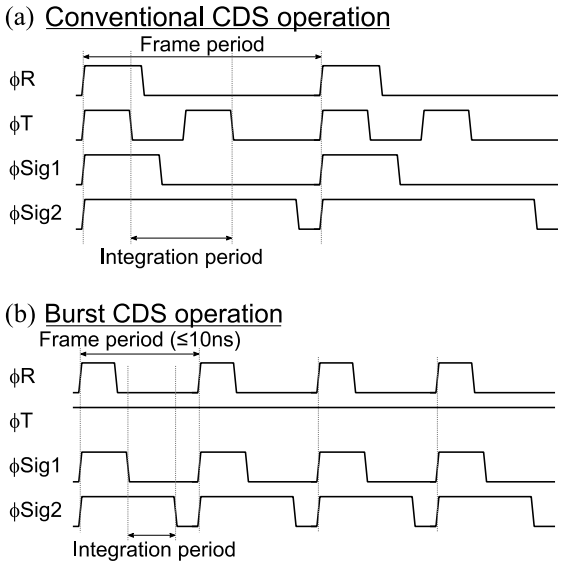


Figure 5 Timing diagram of pixel pulses at (a) conventional CDS operation with switching transfer gate, and (b) burst CDS operation.

realize extremely high frame rate with longer record length. Over 100Mfps with 368 frames imaging by using the developed burst CMOS image sensor is presented.

DESIGN AND STRUCTURE OF DEVELOPED CMOS IMAGE SENSOR

Figure 2 shows the block diagram of the developed CMOS image sensor. The prototype chip has the $50^{H}\times108^{V}$ pixels with in-pixel 368 trench capacitor memory array with 3D stacked equivalent pixel pitch of 35μm. Pixel pulse buffers are arranged in each pixel column, and memory scanning circuit for selecting each frame memory are arranged in each pixel unit row. A vertical and horizontal scan circuits and an analog output buffer are arranged to readout burst video signals.

Figure 3 shows the pixel circuit schematic. It consists of a photosensing unit, a trench capacitor memory array, and a readout circuit. The photosensing unit consists of a 30.00×21.34μm^2 high speed charge collection pinned photodiode (PD) using dopant concentration gradient and fringe electric field[10], a transfer switch (T), a floating diffusion (FD), a reset switch (R), a source follower (SF1), a select switch (X1), a current source (CS1), CDS bypass/select switches, a CDS circuit with a SF buffer (SF2). In-pixel and off-pixel CDS operation are available by using or bypassing the in-pixel CDS circuit. The in-pixel trench capacitor memory array consists of

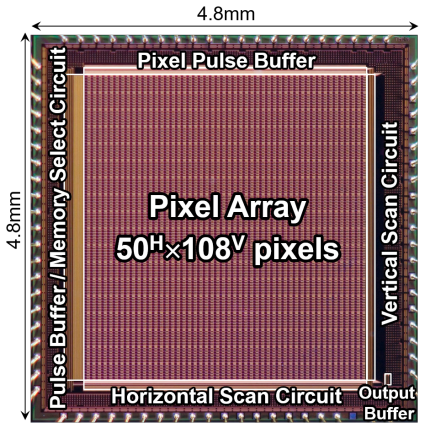


Figure 6 Chip micrograph of the developed burst CMOS image sensor. The number of pixels is extendable.

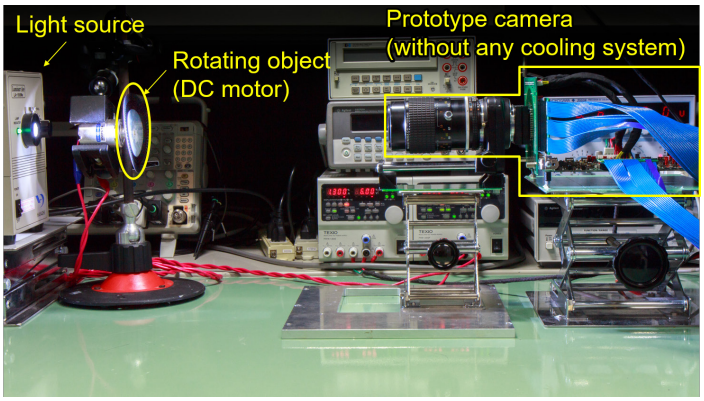
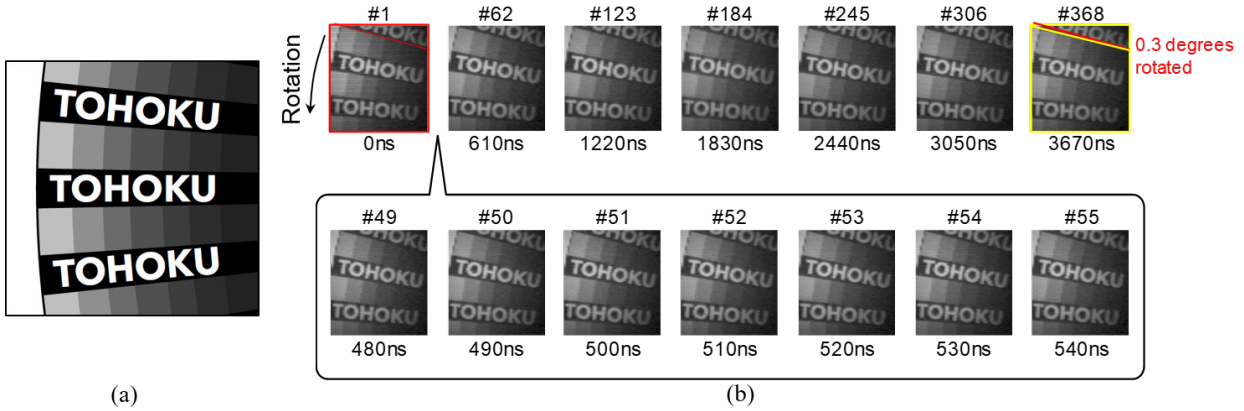


Figure 7 Image capturing setup. The prototype camera has no chip cooling system. Rotating object was illuminated by transmittance light.



(a) (b)

Figure 8 (a) Captured pattern, and (b) sample images of the rotating object (about 13k rpm) captured at 100Mfps 368 frames with in-pixel burst CDS operation mode.

$4^H \times 92^V$ 1-transistor 1-capacitor high density trench capacitor memory cell. A readout circuit consists of four column select switches, a column reset switch (COL_CLR), a write select switch (WS), and a SF with select switch (SF3). During memory signal readout, the WS switch is employed to equalize the input node capacitance of SF3 of each pixel in order to equalize the charge division gain.

Figure 4 (a) depicts the pixel unit arrangement. One unit consists of six pixels in order to address each frame memory per pixel. The memory array is vertically long because the memory select wires need to be routed horizontally. The pixel driving pulse wires run vertically and each pixel output wiring length is made equal in order to equalize the load of the pixel output lines. Figure 4 (b) shows the layout and cross-sectional diagrams of trench capacitor memory. Si trench capacitor with high integrity SiO_2 dielectric film was employed for analog memory to obtain high capacitance with low leakage current and high uniformity[4,5]. The size of the trench capacitor memory cell is $1.4 \times 2.0 \mu m^2$. It achieves about four times higher memory cell density than conventional planar MOS capacitor cell[2-3].

Figure 5 shows the timing diagram of (a) conventional CDS operation and (b) the burst CDS operation[8], respectively. Here, ϕR is pixel reset pulse, ϕT is transfer pulse. ϕSig1 and ϕSig2 are sampling pulses of reset and signal level, respectively. During the burst CDS operation, photoelectrons are always flowing toward the FD due to electric field of about 500V/cm in PD[10], and the bias voltage of the transfer gate was controlled to obtain high conversion gain without potential barrier from PD and FD. The burst CDS technique realizes 10ns frame period or less thanks to minimizing the transition of the pixel driving pulses.

CHIP FABRICATION AND MESUREMENT RESULTS

Figure 6 shows the fabricated chip micrograph. A 0.18μm 1-poly-Si 5-metal-layer CMOS image sensor technology was employed. The chip size is $4.8 \times 4.8 mm^2$. Figure 7 shows the image capturing

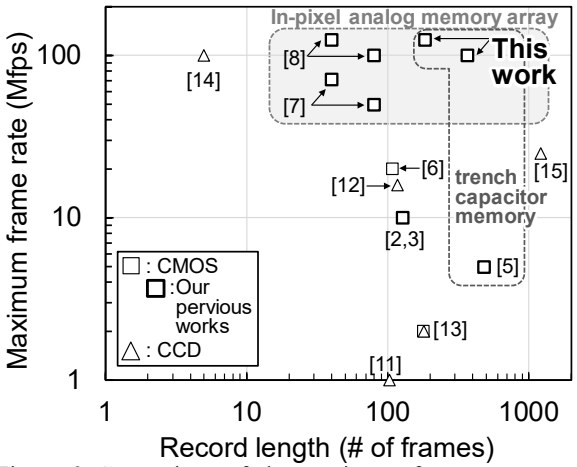


Figure 9 Comparison of the maximum frame rate as a function of record length for the developed chip and recently reported burst image sensors.

Table I. Performance summary of the developed burst UHS CMOS image sensor

Technology	1P5M 0.18 μm CMOS	
Supply voltage [V]	3.3	
Pixel pitch [μm] (3D stacking equivalent)	$70^{H} \times 35^{V}$ $(35^{H} \times 35^{V})$	
Photodiode size [μm^2]	$30.00^{H} \times 21.34^{V}$	
# of pixels	$50^{H} \times 108^{V}$	
# of analog memories/pixel	368	
Maximum frame rate [Mfps]	in-pixel burst CDS mode	off-pixel burst CDS mode
	100	125
Record length	368	184

setup. The prototype camera has no chip cooling systems. Figure 8(b) shows the captured images of a rotating object illuminated by transmitted light. 100Mfps with 368 frames imaging by in-pixel burst CDS operation at room temperature was successfully confirmed with good image quality.

Figure 9 shows the comparison of the maximum frame rate as a function of record length for the recently reported burst image sensors[2–8, 10–15]. The fabricated chip advances the speed and record length performances. Table I summarizes the performances of the developed CMOS image sensor.

CONCLUSION

A global shutter burst CMOS image sensor with in-pixel trench capacitor memory array with over 100Mfps and 368 record length was presented. The developed CMOS image sensor technology can advance the UHS imaging technologies in scientific, engineering and medical fields.

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